

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/671,884	01/10/2001	Shoji Tsuzuki	107927	1918	
25944	7590 11/20/2003		EXAM	EXAMINER	
OLIFF & BERRIDGE, PLC			KEBEDE,	KEBEDE, BROOK	
P.O. BOX 199 ALEXANDRI	928 IA. VA 22320		ART UNIT	PAPER NUMBER	
			2823		
		DATE MAILED: 11/20/2003			

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)				
000 4 4 0	09/671,884	TSUZUKI, SHOJI				
Office Action Summary	Examiner	Art Unit				
	Brook Kebede	2823				
The MAILING DATE of this communication app Period for Reply	ars on the cover sheet with the	correspondence ad	ddress			
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.1 after SIX (8) MONTHS from the mailing date of this communication. If the period for reply specified above is less that theirly (30) days, a reply if the provision of the provisi	36(a). In no event, however, may a reply be till within the statutory minimum of thirty (30) da will apply and will expire SIX (6) MONTHS from cause the application to become ABANDON	mely filed ys will be considered time in the mailing date of this of	ly. ommunication			
1) Responsive to communication(s) filed on 15 Ac	ugust 2003.					
2a) This action is FINAL . 2b) ☐ This	This action is FINAL . 2b)⊠ This action is non-final.					
☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4) Claim(s) 1-16 is/are pending in the application. 4a) Of the above claim(s) 4.10 and 16 is/are wii 5) Claim(s) is/are allowed. 6) Claim(s) 1-3.5-9 and 11-15 is/are rejected. 7) Claim(s) are subjected to. 8) Claim(s) are subject to restriction and/or	thdrawn from consideration.					
Application Papers						
9) The specification is objected to by the Examine	r					
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.						
Applicant may not request that any objection to the						
Replacement drawing sheet(s) including the correct	ion is required if the drawing(s) is of	ojected to. See 37 C	FR 1.121(d).			
11) The oath or declaration is objected to by the Ex	aminer. Note the attached Office	e Action or form P	ΓO-152.			
Priority under 35 U.S.C. §§ 119 and 120						
12) ☒ Acknowledgment is made of a claim for foreign a) ☒ All b) ☐ Some * c) ☐ None of: 1.☒ Certified copies of the priority documents: 2.☐ Certified copies of the priority documents: 3.☐ Copies of the certified copies of the prior application from the International Bureau. * See the attached detailed Office action for a list: 13) ☐ Acknowledgment is made of a claim for domestisince a specific reference was included in the first of the translation of the foreign language pro 14) ☐ Acknowledgment is made of a claim for domestire reference was included in the first sentence of the content of the foreign language pro	s have been received. s have been received in Applical ity documents have been receiv (PCT Rule 17-2(a)). of the certified copies not receiv c priority under 35 U.S.C. § 119 it sentence of the specification cuiv visional application has been re c priority under 35 U.S.C. §§ 120	tion No	application) Data Sheet. a specific			
Attachment(s)						
Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	4) Interview Summar 5) Notice of Informal 6) Other:					

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DETAILED ACTION

Response to Amendment

 The rejection that was mailed on May 15, 2003 withdrawn upon the foreign priority papers translation of said papers has been made of record in accordance with 37 CFR 1.55.

Allowable Subject Matter

 The indicated allowability of claims 5-9 and 11-15 is withdrawn in view of the newly discovered reference(s) to Santadera et al. (US/5,514,613). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

 The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- Claims 1, 2, 5-7, 11, 14, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Santadrea et al. (US/5.514.613).

Re claim 1, Santadrea et al. disclose a method of manufacturing a connection substrate, comprising steps of: forming a metal wire (29) on a base (not shown) (see Col. 4, lines 47-67); applying an insulating material (20 22 24 25) onto the metal wire (29) to form an insulation layer (20 22 24 25); forming another metal wire (21 23 25) on the insulation layer (20 22 24 25), thereby connecting the metal wires which sandwich the insulation layer (20 22 24 25); through a contact hole (not labeled) formed in the insulation layer (20 22 24 25); and separating the metal wires and the insulation layer from the base (not labeled) (see Figs. 1-3; Col. 2, line 59 - Col. 7, line 35).

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Re claim 2, as applied to claim 1 above, Santadrea et al. disclose all the claimed limitations including the limitation wherein the step of applying an insulating material onto the metal wire, and the step of forming another metal wire, thereby connecting the metal wires are repeated at least two times (see Figs. 1-3; Col. 2, line 59 – Col. 7, line 35).

Re claim 5, Santadrea et al. disclose a method of manufacturing a semiconductor device, comprising: a step of forming a connection substrate on a base, comprising, forming a metal wire (29) on a base (not shown), applying an insulating material (20 22 24 25) onto the metal wire (29) to form an insulation layer (20 22 24 25), and forming another metal wire (21 23 25) on the insulation layer (20 22 24 25), thereby connecting the metal wires which sandwich the insulation layer (20 22 24 25) through a contact hole (not labeled) formed in the insulation layer (20 22 24 25); a step of mounting a semiconductor chip on the metal wire which is bared (12A...12M) (see Fig. 3); and a step of separating the connection substrate from the base (see Figs. 1-3; Col. 2, line 59 -- Col. 7, line 35).

Re claim 6, as applied to claim 5 above, Santadrea et al. disclose all the claimed limitations including the limitation wherein a plurality of the semiconductor chips are mounted on the connection substrate (see Figs. 1-3; Col. 2, line 59 – Col. 7, line 35).

Re claim 7, as applied to claim 5 above, Santadrea et al. disclose all the claimed limitations including the limitation wherein in the step of forming a connection substrate, the step of applying an insulating material onto the metal wire and the step of forming another metal wire, thereby connecting the metal wires are repeated at least two times (see Figs. 1-3; Col. 2, line 59 – Col. 7, line 35).

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Re claim 11, Santadrea et al. disclose a method of manufacturing a semiconductor device, comprising: a step of forming a connection substrate on a base, comprising, forming a metal wire (29) to be connected to an electrode (12A...12M) formed on a semiconductor chip (10), on a first base (not shown), applying an insulating material (20 22 24 25) onto the metal wire (29) to form an insulation layer (20 22 24 25), and forming another metal wire (21 23 25) on the insulation layer (20 22 24 25), thereby connecting the metal wires which sandwich the insulation layer (20 22 24 25), through a contact hole (not labeled) formed in the insulation layer; a step of disposing a second base (26) on the connection substrate; a step of separating the first base from the connection substrate; a step of mounting a semiconductor chip on the metal wire that is bared; and a step of separating the connection substrate from the, second base (see Figs. 1-3; Col. 2, line 59 - Col. 7, line 35).

Re claim 14, as applied to claim 11 above, Santadrea et al. disclose all the claimed limitations including the limitation wherein a plurality of the semiconductor chips are mounted on the connection substrate (see Figs. 1-3; Col. 2, line 59 -- Col. 7, line 35).

Re claim 15, as applied to claim 11 above, Santadrea et al. disclose all the claimed limitations including the limitation wherein in the step of forming a connection substrate: the step of applying an insulating material onto the metal, and the step of forming another metal wire, thereby connecting the metal wires are repeated at least two times (see Figs. 1-3; Col. 2, line 59 - Col. 7, line 35).

Claim Rejections - 35 USC § 103

- The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

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the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

 Claims 3, 8, 9, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Santadrea et al. (US/5,514,613) in view of Cronin et al. (US/5,530,262)

Re claim 3, as applied to claim 1 above, Santadrea et al. disclose all the claimed limitations including providing the interconnect on the base and removing the base. However, Santadrea et al. do not specifically disclose a base being glass.

Cronin et al. disclose providing the base (i.e., commonly known as substrate)

(18) (see Figs. 4a --13a) during fabrication metal interconnects. As Cronin disclose, the base such as glass, metal, ceramic, silicon etc. selected so that it can withstand high temperature during device fabrication (see Cronin et al. Col. 5, lines 32-52). So that one of ordinary skill in the art would have motivated to use a base substrate such as glass, metal, ceramic, silicon etc. because it can withstand high temperature during device fabrication.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Santadrea et al. reference with glass base (substrate) as taught by Cronin et al. because the glass substrate would have withstand high temperature during device fabrication.

Re claims 8 and 9, as applied to claim 5 above, Santadrea et al. disclose all the claimed limitations including providing the interconnect on the base and removing the base. However, Santadrea et al. do not specifically disclose a base being glass or silicon.

Cronin et al. disclose providing the base (i.e., commonly known as substrate)

(18) (see Figs. 4a –13a) during fabrication metal interconnects. As Cronin disclose, the base such as glass, metal, ceramic, silicon etc. selected so that it can withstand high

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temperature during device fabrication (see Cronin et al. Col. 5, lines 32-52). So that one of ordinary skill in the art would have motivated to use a base substrate such as glass, metal, ceramic, silicon etc. because it can withstand high temperature during device fabrication.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Santadrea et al. reference with glass or silicon base (substrate) as taught by Cronin et al. because the glass or silicon substrate would have withstand high temperature during device fabrication.

Re claims 12 and 13, as applied to claim 11 above, Santadrea et al. disclose all the claimed limitations including providing the interconnect on the base and removing the base. However, Santadrea et al. do not specifically disclose a base being glass or silicon.

Cronin et al. disclose providing the basc (i.e., commonly known as substrate)

(18) (see Figs. 4a --13a) during fabrication metal interconnects. As Cronin disclose, the base such as glass, metal, ceramic, silicon etc. selected so that it can withstand high temperature during device fabrication (see Cronin et al. Col. 5, lines 32-52). So that one of ordinary skill in the art would have motivated to use a base substrate such as glass, metal, ceramic, silicon etc. because it can withstand high temperature during device fabrication.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Santadrea et al. reference with glass or silicon base (substrate) as taught by Cronin et al. because the glass or silicon substrate would have withstand high temperature during device fabrication.

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Response to Arguments

 Applicant's arguments with respect to claims 1-3, 5-9, and 11-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

- 8. THIS ACTION IS MADE NON-FINAL.
- The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Leedy (US/5,571,741).

Correspondence

- Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-
- 4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kchede

November 15, 2003

W. DAVID COLEMAN